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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,122	01/13/2004	Wai-Fan Yau	AMAT/2592.C7/DSM/LOW K/JW	4554

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,122	YAU ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-13,15-18 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-13,15-18,21 and 23-28* is/are rejected.

7)☒ Claim(s) *22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (U.S. 5,817,572) in view of Sugahara et al. (U.S. 5,989,998).

Chiang et al. (Figs.15-25) teach a method of forming interconnect structures including providing a substrate (320) having a contact (321) formed therein; depositing a first dielectric layer (322) on said substrate; forming an etch stop layer (323) on said first dielectric layer (322); forming a second dielectric layer (350) on said etch stop layer (323); forming a photoresist layer (352) on said second dielectric layer (350); and using said photoresist layer to form a contact hole (351) in said second dielectric layer (350), wherein said first dielectric layer (322) and said second dielectric layer (350) may include any suitable dielectric material or materials including silicon dioxide, silicon nitride, silicon oxynitride, phosphosilicate glass, borophosphosilicate glass, fluoropolymer, parylene, polyimide, any suitable spin-on glass, or any suitable spin-on polymer, and further forming a third dielectric layer (395) over said second dielectric layer (column 13, line 27 – column 16, line 9).

Chiang et al. fail to expressly teach using a low dielectric constant material. However, parylene, polyimide, for example, are known low dielectric constant materials. Therefore, Chiang et al. teach upon the claimed invention.

Chiang et al. fail to teach wherein the low dielectric constant material is a an oxidized organosilane layer, wherein said organosilane layer is deposited in a plasma enhanced process from a mixture comprising an organosilane compound and an oxidizing gas and wherein the carbon content of the low dielectric constant oxidized organosilane layer is form 1% to 50% by atomic weight.

However, Sugahara et al. (Figs.3a-d) teach a method of depositing on a substrate (200) a plurality of layers (202-204), wherein one or more of the layers (202, 204) is a low dielectric constant oxidized organosilane layer comprising carbon, wherein the low dielectric constant oxidized organosilane layer is deposited in a plasma enhanced process from a mixture comprising an organosilane compound an oxidizing gas, wherein said organosilane compound is selected from a phenylsilane group or a vinylsilane group; and etching said one or more of said layers in a patterning process, wherein the carbon content of said oxidized organosilane layer is, for example, 25.7% (first embodiment, chemical formula 2) or 22.2% (ninth embodiment, chemical formula 15) (Sugahara et al., column 7, line 66 – column 8, line 8, line 34, column 8, line 58 – column 11, line 53 and column 18, line 25 – column 21, line 53).

Sugahara et al. fail to expressly teach wherein said oxidized organosilane layer has a carbon content from 1% to 50%. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of

obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dielectric layer with the carbon concentration disclosed in the teachings of Sugahara et al. to arrive at the claimed invention.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chiang et al. and Sugahara et al. to enable forming the SOG layer in Chiang et al. as taught by Sugahara et al. for the further advantage of forming a film with improved film formability, cost efficiency (Sugahara et al., column 3, lines 25 – 30).

3. Claims 15-21 and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (U.S. 5,817,572) in view of Matsuura (U.S. 6,124,641).

Chiang et al. (Figs.15-25) teach a method of forming interconnect structures including providing a substrate (320) having a contact (321) formed therein; depositing a first dielectric layer (322) on said substrate; forming an etch stop layer (323) made of silicon nitride on said first dielectric layer (322); forming a second dielectric layer (350) on said etch stop layer (323); forming a second etch stop layer (390) made of silicon nitride; forming a photoresist layer (352) on said second dielectric layer (350); and using said photoresist layer to form a contact hole (351) in said second dielectric layer (350), wherein said first dielectric layer (322) and said second dielectric layer (350) may include any suitable dielectric material or materials including silicon dioxide, silicon nitride, silicon oxynitride, phosphosilicate glass, borophosphosilicate glass, fluoropolymer, parylene, polyimide, any suitable spin-on glass, or any suitable spin-on

polymer, and further forming a third dielectric layer (395) over said second dielectric layer (column 13, line 27 – column 16, line 9).

Chiang et al. fail to expressly teach using a low dielectric constant material. However, parylene, polyimide, for example, are known low dielectric constant materials. Therefore, Chiang et al. teach upon the claimed invention.

Chiang et al. fail to teach wherein the low dielectric constant organosilane layer is deposited in a plasma enhanced process from a mixture comprising a methylsilane compound and an oxidizing gas, the carbon content of the low dielectric constant oxidized organosilane layer is form 1% to 50% by atomic weight.

However, Matsuura (Figs.1a-4) teaches a method of forming an interconnect layer including forming a low dielectric constant layer (4), wherein the low dielectric constant layer (4) is deposited in a plasma enhanced process from a mixture comprising methylsilane and/or dimethylsilane and an oxidizing gas, the carbon content of the low dielectric constant layer is about 19% by atomic weight (First embodiment, Fig.2), and wherein said oxidizing agents include N_2O and H_2O_2 (Matsuura, column 4, line 17 – column 6, line 65).

Matsuura fails to teach wherein the carbon content of the low dielectric layer is between 1% by atomic weight to 50% by atomic weight. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use to form the layer having said carbon atomic percentage to arrive at the claimed invention.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chiang et al. and Matsuura to enable using the dielectric layer of Matsuura in Chiang et al., for the further advantage of preventing forming a poisoned via in a resulting insulating film (Matsuura, column 2, lines 57 – 64).

Allowable Subject Matter

4. Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (http://portal.uspto.gov/external/portal/pair) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
December 14, 2005

George Fourson
Primary Examiner